CBCS SCHEME

USN | | | | | | | | | | |

21EC32

Third Semester B.E. Degree Examination, June/July 2023
Digital System Design Using Verilog

Time: 3 hrs. Max. Marks: 100

Note: ***Answer any FIVE full questions, choosing ONE full question from each module.***

Module-1

1 a. Define combinational logic circuit and place the following equation into the proper canonical form,

(i) $P = f(a, b, c) = a\bar{b} + a\bar{c} + bc$.

(ii) $Q = f(a, b, c) = (a + \bar{b})(\bar{b} + c)$

(iii) $Z = f(a, b, c, d) = (a + \bar{b})(a + \bar{b} + d)$ **(10 Marks)**

b. Find all the prime implicants of the function using Quine-McClusky method.
$Z = f(a, b, c, d) = \sum m(7, 9, 12, 13, 14, 15) + d(4, 11)$ **(10 Marks)**

OR

2 a. Simplify the following expression using K-map. Implement the simplified expression using basic gates only $F = f(a, b, c, d) = \sum m(0, 1, 2, 5, 6, 7, 8, 9, 10, 13, 14, 15)$. **(10 Marks)**

b. Design a logic circuit that has 4 inputs, the output will be high when the majority of the inputs are high. Use K-map to simplify. **(10 Marks)**

Module-2

3 a. Implement the following Boolean function using 8 : 1 multiplexer and 4 : 1 multiplexer.
$M = f(a, b, c, d) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$ **(10 Marks)**

b. Explain 4-bit carry look ahead adder with neat diagram and relevant expressions. **(10 Marks)**

OR

4 a. Implement full adder and full subtractor using 74138 decoder. **(10 Marks)**

b. Design 2-bit magnitude comparator. **(10 Marks)**

Module-3

5 a. Explain Master Slave JK flip flop with the help of circuit diagram and waveforms. **(10 Marks)**

b. Design a mod-6 synchronous counter using JK flip flop. **(10 Marks)**

OR

6 a. Find characteristic equations for SR, T, D and JK flip flop with the help of function table. **(10 Marks)**

b. Explain four bit binary ripple counter with logic and timing diagram. **(10 Marks)**

Module-4

7 a. List all the data types available in verilog HDL and explain any three data types with examples. **(10 Marks)**

b. Explain various descriptive styles available for hardware modeling using verilog HDL with an example. **(10 Marks)**

OR

8 a. Explain the different types of logical operators with an example program. (10 Marks)
b. Write a full subtractor verilog program using dataflow type of description. (10 Marks)

Module-5

9 a. With a neat block diagram, explain the components of a verilog module by highlighting mandatory blocks. (10 Marks)
b. Write a verilog behavioural code for 4 to 1 multiplexer using case statement. (10 Marks)

OR

10 a. Write a verilog structural code for four bit ripple carry adder. (10 Marks)
b. Explain the highlights of structural description with an example. (10 Marks)

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